

Data Sheet

Product Name	FS8806/FS8826
Date	2007/3/12

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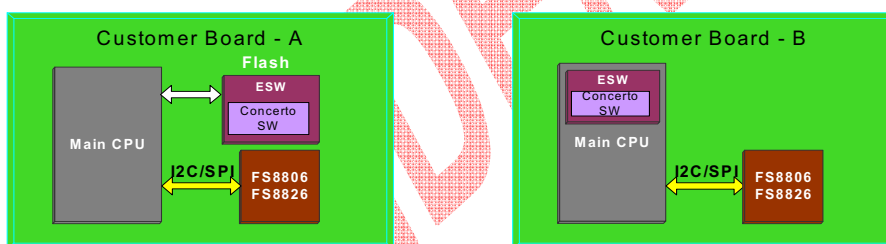
1. Features

- ☐ Secure the authentication and completeness of embedded software
- ☐ Supports I²C and SPI serial interface with secure information exchanged
- ☐ Supports I²C standard mode (100 kbit/s) and fast mode (400 kbit/s)
- ☐ Supports SPI two clock modes, CPOL=0, CPHA=0 and CPOL=1, CPHA=1 under 100 kbit/s or 400 kbit/s.
- ☐ Support 768 bits EEPROM to store user data
- ☐ 8-pin SOP package
- ☐

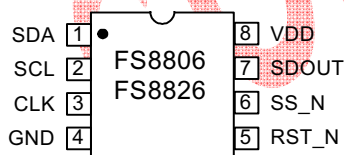
Part Number	CLK Frequency Range
FS8806	1M ~ 10MHz
FS8826	1M ~ 80MHz

2. General Description

FS8806/FS8826 is a companion chip with a solution to authenticate the embedded software license right at the embedded system. It provides a simple and easy solution to implement authentication mechanism in an embedded system. Just connect FS8806/FS8826 with host CPU via I²C or SPI and add pieces of concerto software in original run-time software, then a secure system is ready. The authentication for the embedded software (ESW) license is also very easy. The ESW failed to run in the customer board without FS8806/FS8826 companion or the unmatched FS8806/FS8826 connected with customer board. Two application configurations are shown as below:



3. Connection Diagrams



Pin NO.	Pin Name	I/O	Description
1	SDA	I/O	Open-drain configuration with external pull-up resistor. I ² C serial data or SPI slave data input. 3.3V/5V tolerant.
2	SCL	I/O	Open-drain configuration with external pull-up resistor. I ² C or SPI serial clock. 3.3V/5V tolerant.
3	CLK	I	Clock input. 3.3V/5V tolerant.
4	GND		Ground.
5	RST_N	I	Low active hardware reset. 3.3V/5V tolerant.
6	SS_N	I	Low active SPI slave select. 3.3V/5V tolerant.
7	SDOUT	I/O	Open-drain output with external pull-up resistor. SPI slave data output. 3.3V/5V tolerant.
8	VDD		3.3V VDD.

4. Electrical Secifications

4.1. Absolute Maximum Rating

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	-10	85	$^{\circ}C$
V_{IO}	Input and Output Voltage	-0.5	$V_{CC}+0.5$	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body mode)	-4000	4000	V
V_{ESD}	Electrostatic Discharge Voltage (Machine mode)	-200	200	V
	Latch-up	-200	200	mA

4.2. Operating Condition

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
T_A	Ambient Operating Temperature	0	70	$^{\circ}C$
FS8806 CLK (Note 1,2)	I ² C under 100kbit/s	1	10	MHz
	I ² C 400kbit/s	4	10	MHz
	SPI under 100kbit/s	1	10	MHz
	SPI 400kbit/s	2.5	10	MHz
FS8826 CLK (Note 1,3)	I ² C under 100kbit/s	1	80	MHz
	I ² C 400kbit/s	32	80	MHz
	SPI under 100kbit/s	1	80	MHz
	SPI 400kbit/s	20	80	MHz

Note: 1. Concerto software need to do proper modification when CLK frequency changes.

2. CLK frequency must be more than 10 times I2C/SPI serial clock of FS8806.

3. CLK frequency must be more than 80 times I2C/SPI serial clock of FS8826.

4.3. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	--	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	--	10	pF

4.4. DC Characteristics

Test conditions: (Note1)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{CC}$ or GND	--	0.01	1	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND	--	0.01	1	μA
I_{CC1}	Operating Current	I^2C at 100kbit/s	--	3.3	--	mA
		I^2C at 400kbit/s	--	3.5	--	mA
I_{CC2}	Operating Current	SPI at 100kbit/s	--	3.3	--	mA
		SPI at 400kbit/s	--	3.5	--	mA
I_{SB1} (Note 2)	Standby Current	CLK signal is running	--	160	--	μA
I_{SB2}	Standby Current	CLK signal is stop	--	10	--	μA
V_{IL}	Input Low Voltage	$V_{CC} = 3.3V$	--	--	0.8	V
V_{IH}	Input High Voltage	$V_{CC} = 3.3V$	2.4	--	--	V
V_{OL}	Output Low Voltage	$V_{CC} = 3.3V$	--	--	0.4	V
V_{OH}	Output High Voltage	$V_{CC} = 3.3V$	3	--	--	V

Note: 1. Test condition is as follows:

- FS8806 @ 10MHz CLK Frequency operations
- FS8826 @ 80MHz CLK Frequency operations

2. Standby current for FS8806@10MHz is 160 μA while 580 μA for FS8826@80MHz.

4.5. AC Characteristics

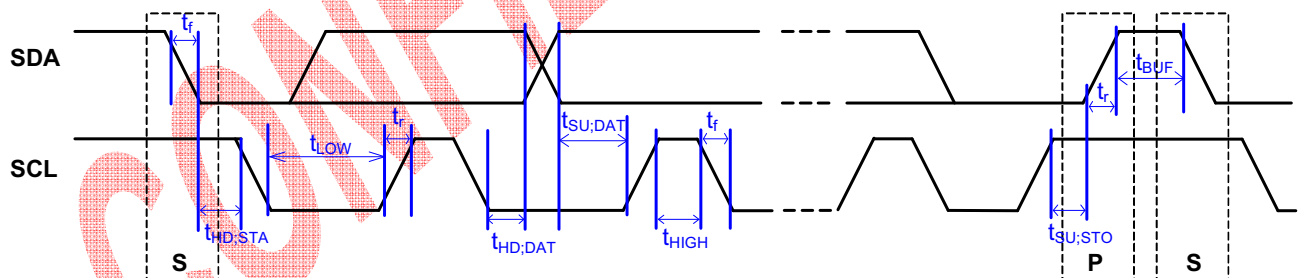
4.5.1. I²C AC Characteristics

Test conditions: (Note1)

Symbol	Parameter	Standard-Mode		Fast-Mode		Unit
		Min.	Max.	Min.	Max.	
f _{SCL}	SCL clock frequency	0	100	0	400	kHz
t _{HD;STA}	Hold time START condition	4.0	--	0.6	--	μs
t _{LOW}	Low period of SCL clock	4.7	--	1.3	--	μs
t _{HIGH}	HIGH period of SCL clock	4.0	--	0.6	--	μs
t _{HD;DAT}	Data hold time	0	3.45	0	0.9	μs
t _{SU;DAT}	Data setup time	250	--	100	--	ns
t _r	Rise time of SDA and SCL	--	1000	20+0.1C _b (Note2)	300	ns
t _f	Fall time of SDA and SCL	--	300	20+0.1C _b (Note2)	300	ns
t _{SU;STO}	Setup time for STOP condition	4.0	--	0.6	--	μs
t _{BUF}	Bus free time between STOP and START condition	4.7	--	1.3	--	μs

Note: 1. Test condition is as follows:

- FS8806 @ 10MHz CLK Frequency operations
- FS8826 @ 80MHz CLK Frequency operations
- 2. C_b = capacitance of one bus line in pF.



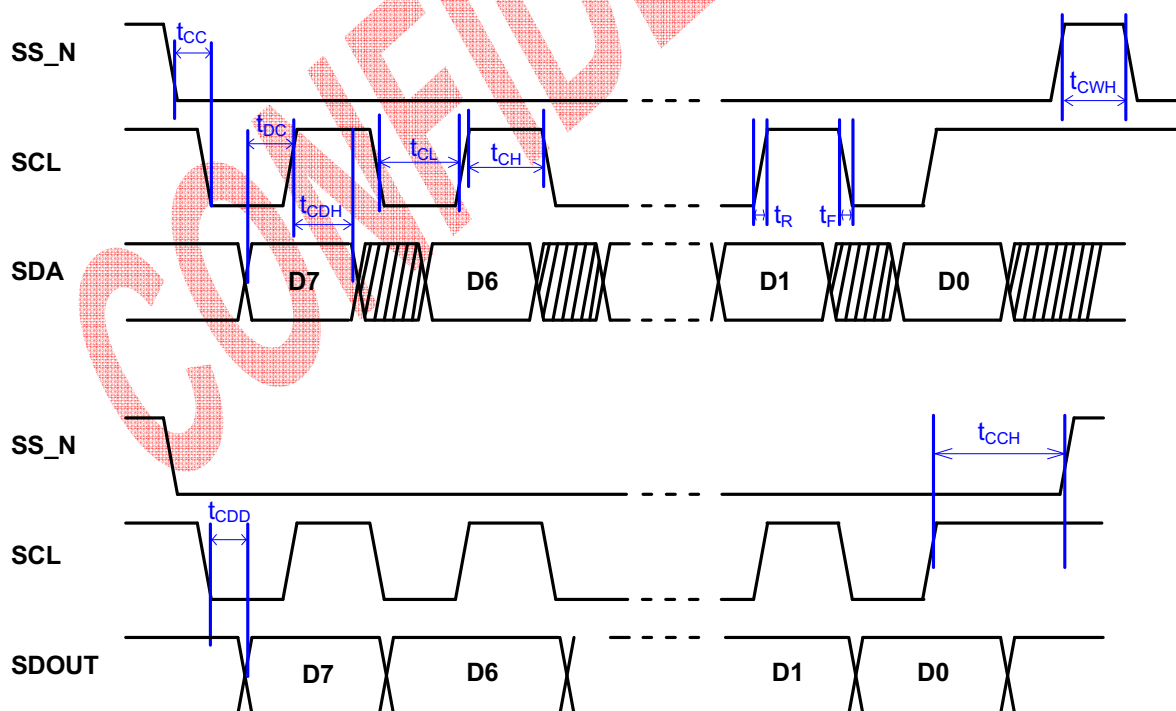
4.5.2. SPI AC Characteristics

Test conditions: (Note1)

Symbol	Parameter	100kHz-Mode		400kHz-Mode		Unit
		Min.	Max.	Min.	Max.	
t_{DC}	Data to SCL setup time	100	--	100	--	ns
t_{CDH}	SCL to Data hold time	100	--	100	--	ns
t_{CDD}	SCL to Data delay	--	200	--	200	ns
t_{CL}	SCL low time	--	5	--	1.25	us
t_{CH}	SCL high time	--	5	--	1.25	us
t_{CLK}	SCL clock frequency	--	100	--	400	kHz
t_R, t_F	SCL rise and fall time	--	100	--	100	ns
t_{CC}	SS_N to SCL setup time	5	--	1.25	--	us
t_{CCH}	SCL to SS_N hold time	5	--	1.25	--	us
t_{CWH}	SS_N inactive time	5	--	1.25	--	us

Note: 1. Test condition is as follows:

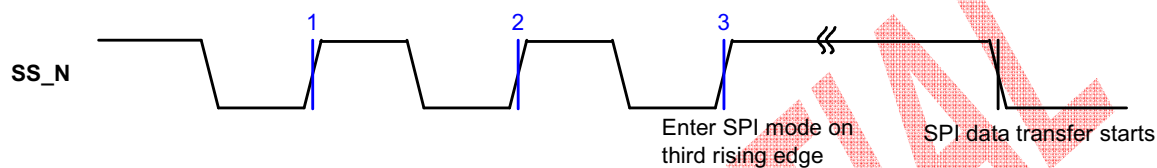
- FS8806 @ 10MHz CLK Frequency operations
- FS8826 @ 80MHz CLK Frequency operations



SCL CAN BE EITHER POLARITY, TIMING SHOWN FOR CPOL=1

4.5.3. SPI Mode Selection

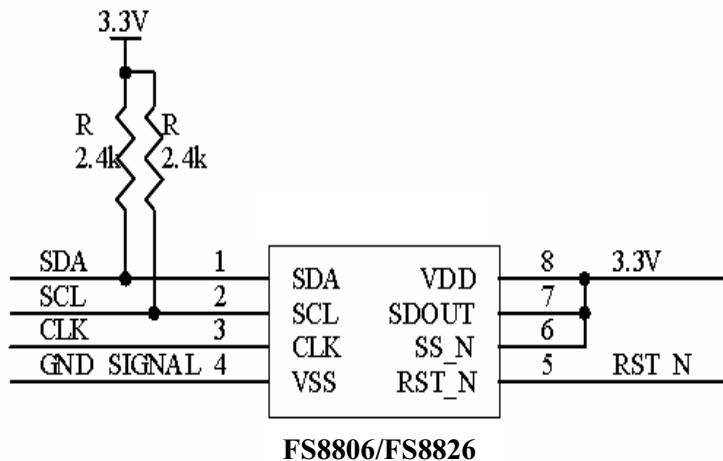
FS8806/FS8826 will operate in I2C mode by default. SPI mode will be entered by receiving 3 rising pulses on SS_N pin after hardware reset. The waveform is shown as below. It will still enter SPI mode if more than 3 rising pulses on SS_N is detected. It is suggested to connect SS_N to power or ground when operating in I2C mode. This serial interface operation mode will be reset only by hardware reset and it will not be changed by software reset.



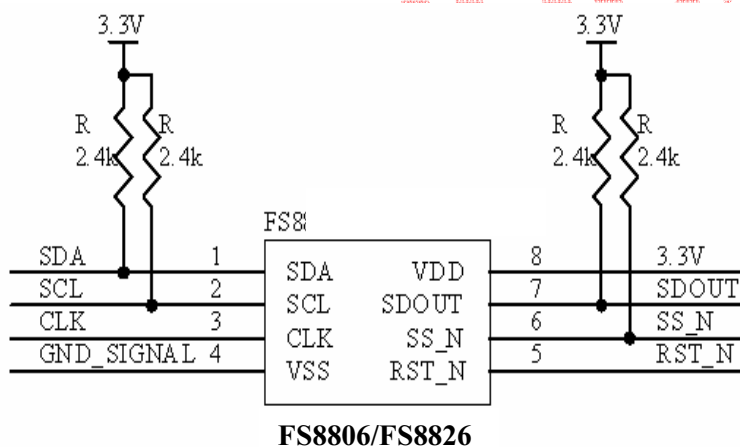
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5. Application Circuit

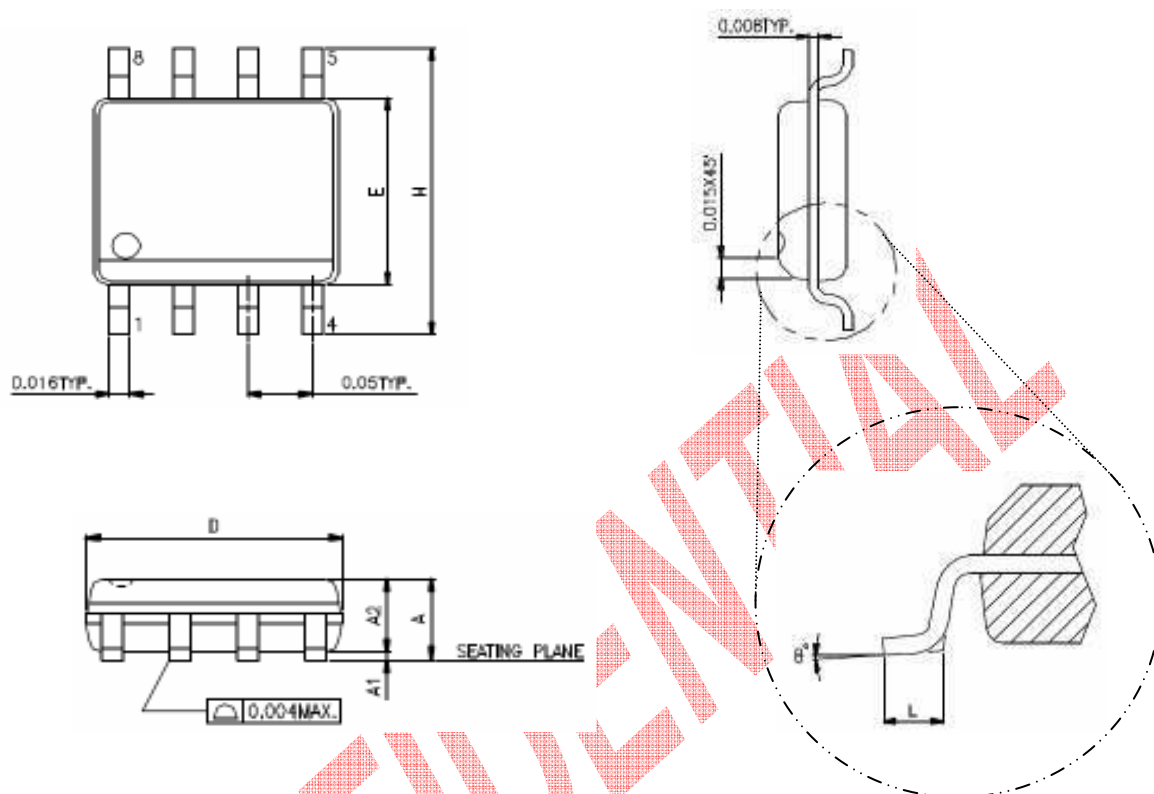
5.1. Only I²C mode



5.2. I²C and SPI mode



6. Package Dimension



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	—	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT: INCH

NOTES:

1. JEDEC OUTLINE: MS-012 AA
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

7. Product Order Information

FS8806 - ESPL

Package Type

ESPL = 8-pins SOP (Non-RoHS)

ESPR = 8-pins SOP(RoHS)

FameG ASoC Device Name

Part Number	Package Type
FS8806ESPL	8-pin SOP Package (Non-RoHS)
FS8806ESPR	8-pin SOP Package (RoHS)
FS8826ESPR	8-pin SOP Package (RoHS)

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8. Revision History

Rev.	Date	Page	Description of Changes
V1.0	March.2006	10	Initial Release
V0.2	March.2006	9	Re-compose
V0.3	March.2006	9	Revise DC Characteristics
V1.0	Mar.28.2006	10	Initial Release to Customers.
V1.1	Aug.29.2006	10	Revise DC Characteristics.
V1.2	Dec.29.2006	10	1. Revise CLK descriptions in DC Characteristics section. 2. Revise page header.
V1.3	Jan.31.2007	12	1. Revise for FS8826 2. Add package dimension
V1.4	Mar.12.2007	12	Revise clock operation and standby current for FS8826 in DC Characteristics section.

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